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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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T. LESTER WALLACE
SILICON EDGE LAW GROUP LLP
6601 KOLL CENTER PKWY, STE 245
PLEASANTON, CA 94566

EXAMINER	
BATAILLE, PIERRE MICHE	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 06/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/855,979	BLIGHTMAN ET AL.	
	Examiner	Art Unit	
	Pierre-Michel Bataille	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5 and 25-27* is/are allowed.

6)☒ Claim(s) *1-4,6-24 and 28-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/19/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is taken in response to Applicant's communication filed March 9, 2005 responding to previous Office Rejection mailed December 17, 2004. Applicant's amendments and/or arguments have been considered with the results that follow.

2. Claims 1-34 are now pending in the application under prosecution as claims 31-34 have been newly added by applicant's amendment.

Response to Arguments

3. Applicant's arguments filed d March 19, 2005 have been fully considered but they are not deemed to be persuasive for at least the following remarks.

Please note that the specification should be amended to reflect the status of all related application, whether patented or abandoned. Therefore, all serial numbers should be updated with respective application number or patent number and their status updated to reflect the current status.

Again, please note that the term "network" in claim 1(e) (second occurrence) is a relative term, which renders the claim indefinite. The claim recites the word "network" in many instances "network" describing "interface device" or "communication". Therefore, the clause 'second portions of data from the network interface device to a network" is not literally clear, as the term '"network" defines other element in the claim. The

specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably appraised of the scope of the invention. It is unclear to what element in the network "outputting the first and second portions of data from the network interface device" refers to.

Claims 1-4, 6-24, and 38-30 were rejected and stand rejected as being anticipated by Applicant's Prior Art. The rejection is maintained based on, at least, the following remarks. Applicant contends that the recited "DMA command queue" differs from "DMA commands 122" of Applicant Admitted Prior Art (AAPA) of Figure 1.

Computer Science Dictionary defines queue as:

a. A sequence of stored data or programs awaiting processing.

b. A data structure from which the first item that can be retrieved is the one stored earliest.

Knowing that Paragraph 0005 of Applicant prior art discloses: processor 109 of Fig. 1 causing DMA controller 115 to execute DMA commands 122 by placing the DMA commands into SRAM 112 where there are thirty-two pending DMA commands 122 stored in SRAM 112; processor 109 instructing the DMA controller to fetch and execute the DMA command by setting a bit in DMA command register 116 wherein the DMA command includes a source address for data to be moved, a destination address for data to be moved, and a byte count. The DMA controller 115 fetching and executing the command, and then setting a corresponding bit in a 32-bit DMA command complete

register 117 corresponding to the 32 pending DMA commands, the DMA command complete register 117 to determine when the DMA command has been completed.

Paragraph 0008 discloses a particular NID (network interface device) 100 of Figure 1 where DMA controller 115 may execute DMA commands in an order different from the order in which the DMA commands were placed in SRAM 112 by processor 109. This statement implies a list of commands being placed in a queue for fetching and execute in a particular order, different from the order from which they were placed in the list.

Moreover, AAPA illustrates queue control as the DMA controller 115 fetching and executing the command, and then setting a bit corresponding to completed DMA command in the DMA command complete register 117; and the processor 109 monitoring the bit in the DMA command complete register 117 to determine when the DMA command has been completed.

In view of above remarks, the rejection with respect to claims 1-4, 6-24, and 28-30 is maintained and repeated below. New claims 31-34 are rejected based on the same arguments, as they do not further define the features of rejected claims 1-4, 6-24 and 28-30.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. Claims 1-4, 6-24, and 28-34 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant Admitted Prior Art (AAPA).

With respect to claim 21 and 28-31, Applicant Background Art teaches the invention as claimed, an apparatus as described in ***Prior Art Fig. #1 and paragraphs 0003 to 0008***, implementing the method comprising: a DMA command queue ***(DMA Commands 122)*** to ensure that a plurality of DMA moves are completed in a particular sequence ***(DMA controller may execute DMA commands in an order different from the order the DMA commands were placed)***, each of the DMA moves being a move of information from one location on a network interface device to another location on the network interface device ***(moves of first, second and third portions from host storage 121 to DRAM 106)***, the DMA command queue being maintained by queue manager hardware on the network interface device **(Queue manager hardware 108 on the network interface device (NID) 100)**, the DMA moves being carried out by a DMA controller, the DMA controller being a part of the network interface device ***(DMA controller 115 being part of the* network interface device (NID) 100*)***; and outputting at least part of the information from the network interface device ***(transmission of data packet)***.

With respect to claims 22-23, Applicant Background Art teaches the invention as claimed, the information outputted from the network interface device to a host computer,

the host computer coupled to the network interface device ***(packet outputted from the network interface device (NID) 100 coupled to host computer 101 or network 102 in the form of data payload) [Par. 0004 & 0008]***.

With respect to claims 24 and 32, Applicant Background Prior Art teaches the invention wherein a first of the plurality of DMA moves is a move of at least a part of a frame of a session layer message, and wherein a second of the plurality of DMA moves is a move of at least a part of a subsequent frame of the session layer message ***[NID including physical layer interface circuitry 105 with the NID completing the moves of first, second and third portions in a sequence, Par. 0003 & 0008]***.

With respect to claim 1, Applicant Background Prior Art teaches the invention as claimed, a method, comprising: maintaining on a network interface device a DMA command queue ***[NID 100 with command queue 122 in SRAM 112]***; processor on the network interface device causing a value to be pushed onto the DMA command queue, the value being indicative of corresponding DMA command ***[processor 109 placing DMA commands Par. 0008]***; popping a value off the DMA command queue ***[Par. 0005]***, a DMA controller on the network interface device then executing a DMA command indicated by the popped value ***[DMA CTRL 111 executing DMA Commands, Par. 0005]***; repeating and such that a first portion of data is transferred from host storage to a local memory on the network interface device and such that a second portion of data is transferred from the host storage to the local memory on the

network interface device ***[Par. 0007]***; and after both the first portion and the second portion are present the local memory, outputting the first and second portions of data from the network interface device to a network, the first and second portions making up at least a part of a data payload of a network communication ***[Par. 000008]***.

With respect to claim 2, Applicant Background Prior Art teaches maintaining a DMA command complete queue on the network interface device ***[DMA command complete queue 17]***, the DMA controller pushing values onto the DMA command complete queue, the processor popping values off the DMA command complete queue ***[Par. 0007]***.

With respect to claim 3, Applicant Background Art teaches the system and method wherein the processor uses the DMA command complete queue to determine that the first and the second portions of data are both present in local memory on the network interface device ***[DRAM local memory 106; Par. 0007]***.

With respect to claim 4, Applicant Background Art teaches the system wherein the network interface device comprises queue manager hardware ***[Queue MNGR 108]***, the queue manager hardware maintaining the DMA command queue in static random access memory (SRAM) ***[SRAM 112]***, wherein the processor, the queue manager hardware ***(108)***, the SRAM ***(112)***, and the DMA controller ***(115)*** are all part of the same integrated circuit ***[Network Interface Device 100]***.

With respect to claims 6-8, Applicant Background Art teaches the system wherein each of the values on the DMA command queue is a DMA command; each of the values on the DMA command queue comprises a pointer a DMA command; and each of the values on the DMA command queue is a number that identifies location where a DMA command is stored ***[Par. 0005]***.

With respect to claims 9-10 and 33, Applicant Background Art teaches the system wherein: the network interface device an expansion card ***(NIC 100)*** coupled to a host computer ***(101)***, the host storage ***(121)*** being part of the host computer ***(101)***; the network interface device a part of a host computer ***(101)***.

With respect to claims 11 and 34, Applicant's Background Art in Fig. 1 discloses the invention as claimed, a network interface device ***(100)*** comprising: queue manager hardware ***[QUEUE MNGR 108]*** that maintains a DMA command queue ***[DMA command queue 122 in SRAM 122]***; a processor ***(109)*** coupled to the queue manager hardware (108), the processor causing values to be pushed onto the DMA command queue ***[Par. 0005]***; DMA controller ***(115)*** coupled to the queue manager hardware ***(108)***, the DMA controller executing DMA commands, the DMA commands executed being indicated by values popped off the DMA command queue ***[Par. 0005]; local memory DRAM local memory 106]*** that temporarily stores a first portion data transferred by execution of one or more DMA commands from data storage on a host

coupled to the network interface device into the local memory, the local memory ***(106)*** also temporarily storing a second portion of data transferred by execution of one or more DMA commands ***(DMA command 122)*** from the data storage ***(121)*** on the host to the local memory ***(106) [Par. 0006 & 0007)***; and physical layer interface ***(105)*** and media access control circuitry ***(107)***, the physical layer interface ***(105)*** and media access control circuitry ***(107)*** outputting the first and second portions data from the network interface device network, the first and second portions of data being output in the form of a data payload of a network communication ***[Par. 0004]***.

With respect to claims 12-13, Applicant's Prior Art discloses the network interface device wherein the local memory is dynamic random access memory ***(DRAM 106)***, and the queue manager hardware stores at least part of the DMA command queue ***(122)*** in static random access memory ***(SRAM 112) [Par. 0005]***.

With respect to claims 15-16, Applicant's Prior Art discloses the network interface wherein the processor outputs the first and second portions of data in a network ***[network 202]***; and wherein the processor outputs the first and second portions data in a host computer ***(Host 101) [Par. 0008]***.

With respect to claims 17-20, Applicant's Prior Art discloses the network interface wherein: the first place is a dynamic random access memory ***(DRAM 106)*** and wherein the second place is a bus interface ***[PCI BUS INT. 114]***; the first place is bus interface

[PCI BUS INT. 114] and wherein the second place is a dynamic random access memory ***(DRAM 106)***; the first place is bus interface ***[PCI BUS INT. 114]*** and wherein the second place is a static random access memory (SRAM) ***(SRAM 112) [Par. 0005]***; and the first place is a static random access memory ***(SRAM 112) [Par. 0005]***. and wherein the second place is a bus interface ***[PCI BUS INT. 114]***.

Allowable Subject Matter

6. Claims 5 and 25-27 are allowed.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre-Michel Bataille whose telephone number is (571) 272-4178. The examiner can normally be reached on Mon-Fri (9:30A to 6:00P).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Pierre-Michel Bataille
Primary Examiner
Art Unit 2186

May 28, 2005

PIERRE BATAILLE
PRIMARY EXAMINER